taxial layer **110**. N-type region **125** is a ring shaped region that surrounds base region **130**. N-type region **125** is a deep n+ region formed in epitaxial layer **110** in the active area that forms a low resistance path from a surface of epitaxial layer **110** to buried layer **115**. A heavily doped n-type region **135** is formed in region **125** that couples to terminal **15** of ESD protection circuit.

[**0011**] Zener diode **30** of **FIG. 1** comprises a p-type region **150**, epitaxial layer **110**, and n-type region **125**. P-type region **150** overlies a boundary of base region **130** and epitaxial layer **110**. P-type region **150** couples to base region **130** and is formed in a ring shape around the periphery of base region **130**. P-type region **150** has a higher doping concentration than base region **130**. As shown in **FIG. 1**, zener diode **30** is coupled in parallel with the collector-base of transistor **25**. The spacing between p-type region **150** and n-type region **125** and the doping concentrations of the device components of zener diode **30** play a role in determining what voltage zener diode **30** breaks down.

[**0012**] Resistor **35** of **FIG. 1** corresponds to the inherent resistance of base region **130**. In an ESD event, impact ionization current is generated by zener diode **30** when the breakdown voltage of zener diode **30** is exceeded. The impact ionization current is coupled to base region **130**. Note that both emitter region **145** and p-type region **140** are coupled to ground through terminal **20** of ESD protection circuit **10**. The inherent resistance of base region **130** produces a voltage drop as impact ionization current is conducted that forward biases the base-emitter junction of transistor **25**. Upon enabling transistor **25**, a portion of the impact ionization current is base current for the device. The base current is multiplied by the current gain of transistor **25** which rapidly dissipates the energy of the ESD event and clamps the voltage from exceeding a value that can damage circuitry coupled to terminal **15**. The voltage at terminal **15** falls as transistor **25** dissipates the energy of the ESD event. Zener diode **30** stops conducting current when the voltage at terminal **15** falls below the breakdown voltage of the device. Transistor **25** is disabled when deprived of the current from zener diode **30** thus returning to the state prior to the ESD event with no current being conducted by zener diode **30** and transistor **25**.

[**0013**] **FIG. 3** is a graph of a transmission pulse line characteristic corresponding to ESD protection circuit **10** of **FIG. 2**. Transmission pulse line testing provides a pulse similar to an ESD event to an ESD protection circuit. The voltage and current coupled to the ESD protection circuit is monitored. A curve on the graph relates to measurements on an ESD protection circuit similar in structure to that shown in **FIG. 2** and measuring 52.5 microns on a side. Voltage is displayed on the x-axis and current on the y-axis.

[**0014**] The voltage impulse is clamped to a voltage magnitude less than 50 volts as the zener diode breaks down providing impact ionization current to enable the transistor. The voltage rapidly falls to approximately the breakdown voltage of the zener diode plus a base-emitter junction voltage. The test equipment measures the maximum current that can be handled by ESD protection circuit before failure. The point of failure is represented by dot **210** on the curve which corresponds to a current slightly less than 4000 milliamperes.

[**0015**] Although not indicated by the graph, the failure mechanism typically results in damage at the base terminal of the ESD protection circuit. As mentioned previously, the transistor tested corresponds to the device shown in **FIG. 2**. The transistor tested is a vertical device comprising emitter region **145**, base region **130**, and epitaxial layer **110** (collector). The device structure shown also has parasitic lateral transistor component that is inherent to the design. It is believed that the failure at the base terminal of the device occurs due to high currents flowing near the surface of the transistor due to currents from the zener diode and the lateral transistor that couple to the base terminal. An ESD event of substantial energy produces a current at the base terminal due to the circuit structure that causes a failure in the ESD protection device.

[**0016**] Accordingly, it is desirable to provide an electrostatic discharge protection circuit capable of suppressing higher energy electrostatic events. It would be beneficial if the electrostatic discharge protection circuit had a smaller footprint. It would be of further benefit if the electrostatic discharge protection circuit did not require any special manufacturing steps. Furthermore, other desirable features and characteristics of the present invention will become apparent from the subsequent detailed description and the appended claims, taken in conjunction with the accompanying drawings and the foregoing technical field and background.

BRIEF DESCRIPTION OF THE DRAWINGS

[**0017**] The present invention will hereinafter be described in conjunction with the following drawing figures, wherein like numerals denote like elements, and

[**0018**] **FIG. 1** is a schematic diagram of a prior art electrostatic discharge circuit;

[**0019**] **FIG. 2** is a cross-sectional view of a prior art electrostatic discharge (ESD) protection circuit corresponding to the schematic diagram of **FIG. 1**;

[**0020**] **FIG. 3** is a graph of a transmission pulse line characteristic corresponding to the ESD protection circuit of **FIG. 2**;

[**0021**] **FIG. 4** is a cross-sectional view of an electrostatic discharge (ESD) protection circuit in accordance with the present invention;

[**0022**] **FIG. 5** is a graph of a transmission pulse line characteristic corresponding to ESD protection circuit of **FIG. 4**; and

[**0023**] **FIG. 6** is a top view of an ESD protection circuit in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[**0024**] The following detailed description is merely exemplary in nature and is not intended to limit the invention or the application and uses of the invention. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding technical field, background, brief summary or the following detailed description.

[**0025**] A zener diode triggered bipolar transistor electrostatic discharge (ESD) protection circuit similar to that shown in **FIG. 1** is capable of being formed on both existing and future wafer process flows. In general, cost is a factor in